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Development of power electronic distribution transformer using fuzzy logic control

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A B S T R A C T

This paper presents the design and analysis of power electronic distribution transformer (PEDT). The PEDT is the new distribution transformer based on power high-frequency transformer and electronic converter. Operating the PEDT with the conventional proportional integral (PI) control does not give a satisfactory dynamic response and power quality. Improved power quality dynamic performance of PEDT can be achieved by using intelligent control. This study proposed a novel controller for a PEDT based on fuzzy logic control (FLC). The performance and power quality of the proposed PEDT are improved by replacing the conventional PI controller with the modern FLC. The proposed model was simulated using MATLAB/Simulink in order to evaluate the behavior of the PEDT. The model was tested under the study state and transient state. The results show that the PEDT with the proposed FLC gives a better dynamic performance and power quality compared to the PI controller.

1. Introduction

The power-electronic distribution transformer (PEDT) also referred as the solid-state transformer is a new transformation device based on the power electronics on both primary and secondary sides. It is considered as one of the ten most emerging technologies by the Massachusetts Institute of Technology (MIT), technology review (She et al., 2012). The PEDT is proposed to replace the conventional line-frequency transformer, aimed to overcome the limitation of the current distribution transformers. The conventional line-frequency transformer lacks the capability of energy storage, power quality improvement and, transient disturbance compensation.

The first power electronic transformer was proposed by William (1970) and since then many research studies on PEDTs have been carried out which focused on the design and control of the PEDT (Hariri, 2015; Wang et al., 2016). There are two main approaches for designing power electronic distribution transformers; the first one is based on an AC link (Kang et al., 1999; Aijuan et al., 2006; Basu and Mohan, 2014). In this design model, the transformer size, weight, and stress factor are reduced noticeably, but the drawback of this method is the difficulty to implement feedback control and power factor improvement. The second approach is based on the DC link which has many attractive features as used in this project (Zhao et al., 2013; Zhang et al., 2014; Madhusoodhanan et al., 2015, Ahmed et al., 2017). The topology prevents propagation of voltage or current harmonics on one side of the transformer to another side; this makes the model more suitable for non-linear load applications with improved power factor. This model will probably be the mainstream of the future PEDT. In this paper, the control of PEDT was improved by replacing the inner current loop, PI controller by an FLC. The proposed novel control strategy based on the fuzzy controller realizes good dynamic performance, unity power factor and less total harmonic distortion (THD). The result shows that the PEDT do not only stepped the voltage to a lower level as the conventional transformer but also improved the power quality of the system, which can widen the application range of the PEDT.

2. Operating principle and modelling of the PEDT

The basic configuration of the proposed PEDT is shown in Fig. 1. It includes three parts: The input stage, which is utilized to correct the input power factor, to reduce the THD on the grid side, and to adjust the primary DC bus voltage as a reference. The

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isolation stage is a second part, which provided the galvanic isolation between the primary and secondary side. In this part, the DC voltage is converted to a high-frequency (HF) square-wave signal by HF converter, connected to the primary of HF transformer. The HF square-wave voltage step-down by HF transformer and then rectified back to DC voltage by the second HF converter. The last part is an output stage, which inverters the DC voltage to AC voltage with line frequency 50 Hz.

The input stage is implemented by a three-level, three-phase PWM rectifier phase. The three-phase *abc*-frame model for the PWM rectifier can be expressed as follows:

$$e_i = L\frac{di_i}{dt} + Ri_i + S_{i1}v_{dc1} - S_{i2}v_{dc2} + u_{no} \quad (1)$$

where i *is a,b,c,* and e_i are the three-phase input AC voltages and L and R are the input inductance and resistance respectively between the grid and the converter, V_{dc1} and V_{dc2} are the capacitance DC voltage, i is the rectifier output current, C_d is the DC link capacitor, S_i are the switching functions and u_{no} is voltage between grid neutral point and three-level rectifier neutral point on DC side.

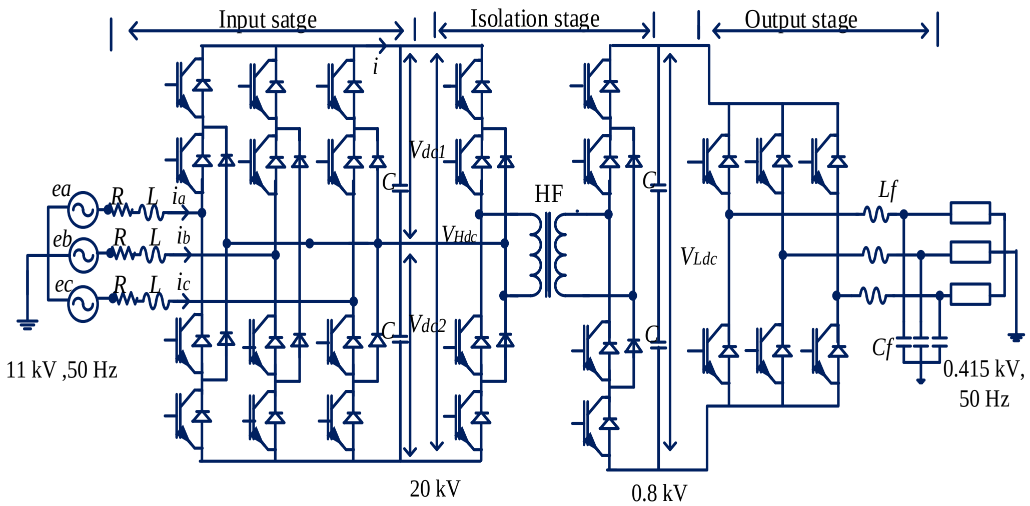

Fig. 1: Proposed topology of the PEDT

For modelling and designing of the controller, it is very useful and suitable to convert the three-phase a, b, c variables into a rotating d-q frame, this reference frame theory is well-known to electrical engineers as Park's transformation (Krause et al., 2013). The mathematical model of the three-level PWM rectifier in the two-phase synchronous rotation d-q coordinate is:

$$L\frac{di_d}{dt} = -Ri_d + \omega Li_q - S_{d1}v_{dc} + S_{d2}v_{dc} + e_d \quad (2)$$

$$L\frac{di_q}{dt} = -Ri_q - \omega Li_d - S_{q1}v_{dc} + S_{q2}v_{dc} + e_q \quad (3)$$

and the DC capacitor voltages are:

$$C_d\frac{dv_{dc1}}{dt} = \frac{3}{2}(S_{d1}i_d + S_{q1}i_q) - i \quad (4)$$

$$C_d\frac{dv_{dc2}}{dt} = -\frac{3}{2}(S_{d2}i_d + S_{q2}i_q) - i \quad (5)$$

The isolation stage of PEDT consists of a high voltage half bridge three level converters and low voltage half-bridge converter with a high-frequency transformer in between. The power flows from the primary converter with a leading phase angle to the secondary converter with lagging phase angles, the amount of the transferred power being controlled by the phase shift between the two square wave voltage, and the DC link voltages magnitudes at the two ends as given by Eq. 6 (Alepuz et al., 2014):

$$P_o = \frac{V_{Hdc}V_{Ldc.}\emptyset(\pi - |\emptyset|)}{\pi\omega L} \quad (1)$$

where V_{Hdc} is the high voltage DC link, V'_{Ldc} is the low voltage DC link referred to the high voltage side, L is the leakage inductance, $\omega = 2\pi f_w$, f_w is the switching frequency, and ϕ is the phase shift of the PWM signal between the primary and secondary sides.

The output stage is two-level half-bridge converter connected with HF transformer. The mathematical model of the output stage was similar to the input stage, and the same model described in the input stage, Eqs. 2-4 can be properly applied to the output stage so no difference exists between the HV and the LV side converters apart from the involved variables.

3. Fuzzy logic controller

Fuzzy logic control has rapidly become one of the greatest successful controllers for developing sophisticated control systems. Various researchers have devised advanced control techniques for power electronics circuits based on fuzzy logic. The FLC incorporates attractive features such as simplicity, low-cost hardware, and software implementation and provides good dynamic performance. The FLC consists of two inputs and one output u. The first input is the error e(k); it is the difference between the reference and measure voltage as in Eq. 8, and the second input is the change of error Ce(k) as given in Eq. 9 and is shown in Fig. 2.

$$e(k) = i_{ref}(k) - i_{dc}(k) \quad (2)$$

$$Ce(k) = e(k) - e(k-1) \quad (3)$$

The main FLC characteristics are:

- Five membership functions are used for the two inputs and one output.
- The type of membership function is Triangular.
- Fuzzification uses a continuous discourse.
- Mamdani min operator is used as the Implication.
- Defuzzification uses the centroid method.

The FLC structure uses the error of the converter circuit as the two inputs (error and change of error) and has one output as present in Fig. 3. The output of the FLC generates a PWM signal which used to drive the semiconductor switching.

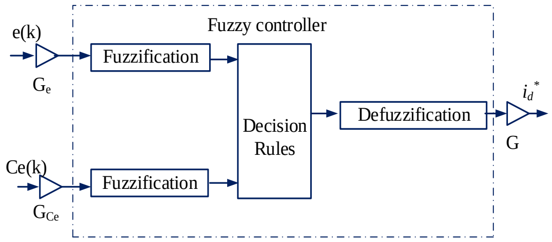

Fig. 2: DC voltage regulation based on fuzzy controller

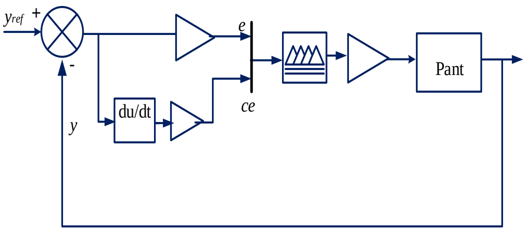

Fig. 3: Basic block diagram of FLC

All fuzzy control membership functions have the same variables. Five membership functions are used for the two inputs and one output named from negative big (NB) to positive big (PB) as listed in Table 1.

Table 1: Fuzzy rules

Δe/e	NB	NS	Z	PS	PB
NB	NB	NB	NB	NM	Z
NS	NB	NM	NS	Z	PM
Z	NB	NS	Z	PS	PB
PS	NM	Z	PS	PM	PB
PB	Z	PM	PB	PB	PB

4. Control design for the PEDT

The output stage control designed is based on Eqs. 4-7 as shown in Fig. 4. The output DC voltage is compared to the reference voltage in order to implement the control for the outer voltage loop to ensure constant voltage in the DC link. The difference passes through the FLC to generate the inner current i_d reference value, while the i_q reference is set to zero; this is to realize the unity power factor. The three-phase input currents in the inner current loop are converted into d-q axis current components. The d-q axis currents are compared with the reference values of both d-q axis current and the differences pass the FLC to control the inner current loop to improve the power factor and provide less harmonic distortion.

4.1. The isolation stage control

The low voltage DC link regulated by phase shift control as shown in Fig. 5 and the power also controlled according to (10). The DC voltage compares with the reference voltage the error pass through FLC to generate the PWM signal.

4.2. The output stage control

The output stage closed-loop control scheme is shown in Fig. 6. The output voltages e_{do} e_{qo}, compared with the reference values of e_{do}^* and e_{qo}^* the error passes FLC to generate the modulated signal for PWM. The PWM control algorithms realize the control of inverter switches.

5. Results and discussion

In order to evaluate the performance of the proposed power electronic distribution transformer and the FLC, the overall system was implemented in MATLAB/Simulink. Moreover, the main simulation parameters of the PEDT are given in Table 2.

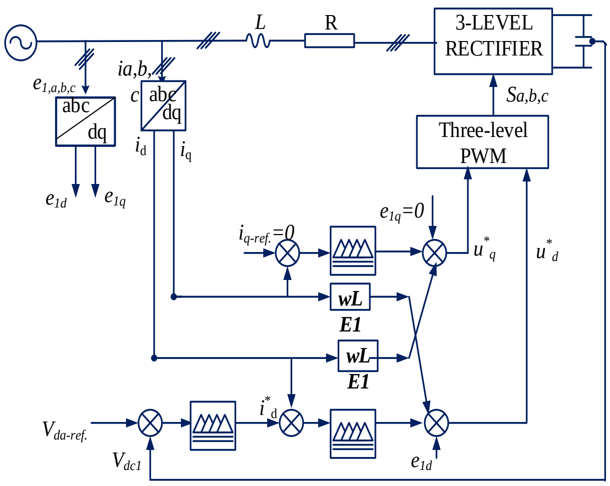

Fig. 4: Input stage control of the PEDT

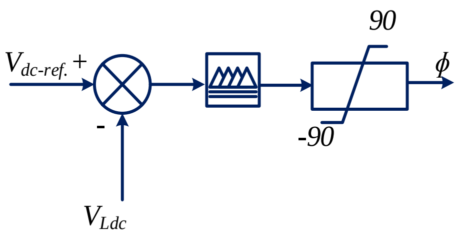

Fig. 5: The isolation stage control

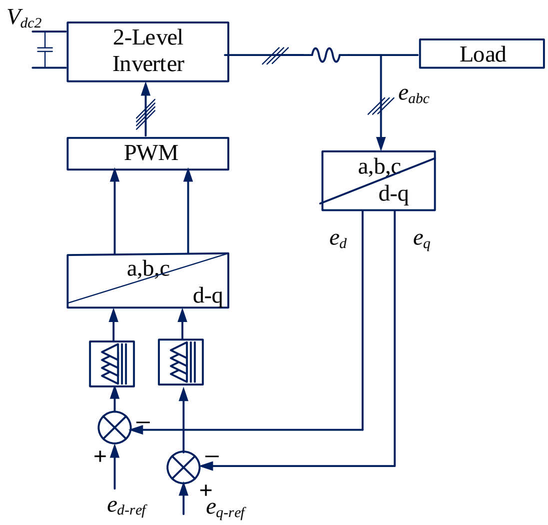

Fig. 6: The output stage control

Table 2: PEDT specifications

Parameter	Value
Transformer power rating	100kVA
Input voltage (L-L)	11kV
Output voltage (LL)	415
Input resistance and inductance	0.07 Ω, 237mH
High DC link capacitance	20μF
High voltage DC link	20 kV
Low DC link capacitor	20mF
Low voltage DC link	800 V
Isolation stage switching frequency	10kHz
Output filter	4mH,30kvar
Load	90kW ,40kvar

5.1. Steady state results

The steady state performance of the proposed PEDT is investigated under the rated condition and presented in Figs. 7-12 for the conventional PI controller and the proposed FLC. Figs. 7 and 8 present the simulation results for the input and output voltages and currents. The voltage and current were clearly sinusoidal and in phase, indicating that there was less THD and near unity power factor was achieved on the grid and load sides. The THD of the input current for bother controller are shown Figs. 9 and 10. The THD for the proposed FLC controller was 1.98% while the THD for the conventional PI controller 2.42%. The FLC give better harmonic distortion, this is due to the proposed controller capability for improving the power quality.

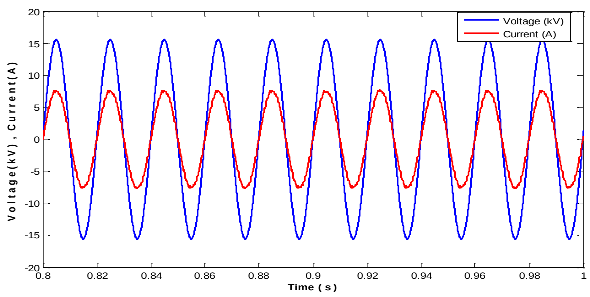

Fig. 7: Input voltage and current for phase A

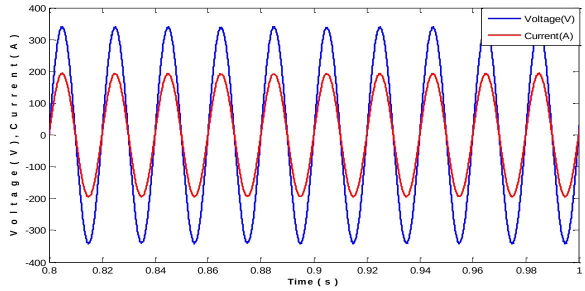

Fig. 8: Output voltage and current for phase A

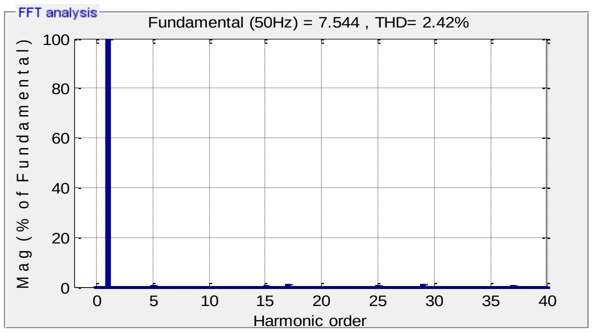

Fig. 9: THD for the input current with PI controller.

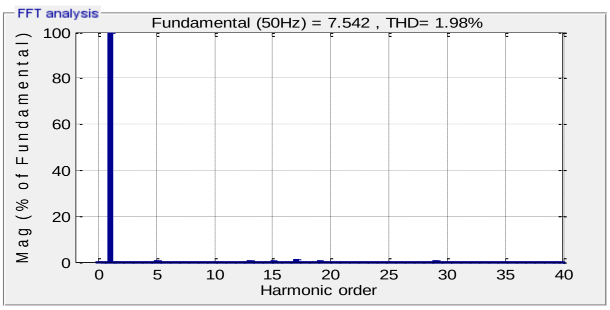

Fig. 10: THD for the input current with FLC

High DC link voltage of PI controller and FLC is presented in Fig. 11. It shows that the high DC voltage was equal to 20kV as adjusted to the reference voltage by the input stage controller. Further, Fig. 12 shows the low DC voltage link, and it was 800 V as the reference value. The response of both controllers was the same in the steady state condition.

Table 3 summarized the steady state results of the PEDT for both controllers, and they were almost the same, except for the THD; the FLC gave better harmonic distortions compared to the conventional PI controller.

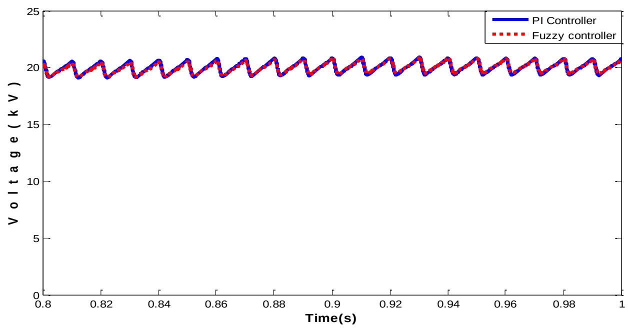

Fig. 11: PEDT high voltage DC link

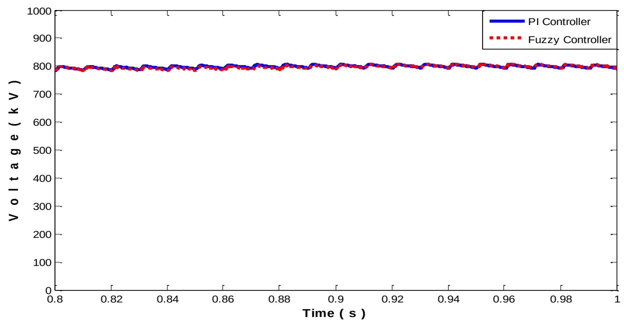

Fig. 12: PEDT low voltage DC link

Table 3: Results of the PEDT

Parameter	FLC	PI controller
High voltage DC Link	20 kV	20 kV
Low voltage DC Link	800 V	800 V
Output phase voltage of the proposed PEDT	240 V	240 V
Output Current	140 A	140 A
Output frequency	50 Hz	50 Hz
The input power factor	0.998	0.995
THD in the grid side	1.98%	2.42%

5.2. Voltage sag

The dynamic response of the PEDT when the voltage sag supplied on the primary side of the PEDT is presented from Figs. 13-16. The input voltage and current presented in Fig. 13 when a 30 V sag is applied from 1.2s to 1.3s. The output voltage and current waveforms are presented in Fig. 14 as it is evidenced they were not affected by the input voltage sag; this indicated that the PEDT controller compensates the voltage sag without propagating to the secondary side. In addition, the voltage and current were in phase and almost sinusoidal.

Fig. 15 shows that the high voltage DC bus for the PI controller varied between 18.5 kV and 22.4 kV, but the DC based on the proposed FLC varied slightly between 19.3 kV and 20.8 kV, but the difference is relatively small and negligible. Also, from Fig. 16, it is seen that the lower DC voltage based on the PI controller varied around 0.8kV, but the DC voltage based on the FLC remained constant at the reference voltage. Moreover, the response obtained by the FLC when the voltage sag happened was better than the PI controller.

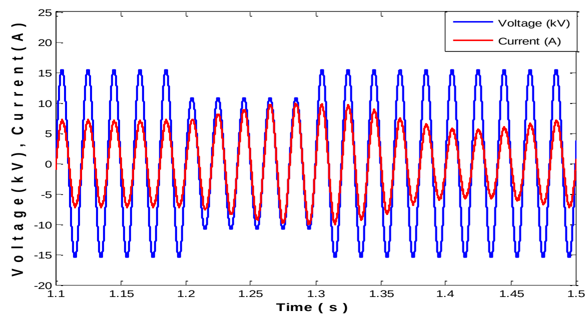

Fig. 13: PEDT Input voltage and current under voltage sag

The results show that the FLC has a better dynamic response and total harmonic distortions compared to the traditional PI controller. The simulation results for voltage sag are tabulated for comparative performances between the two controllers in Table 4.

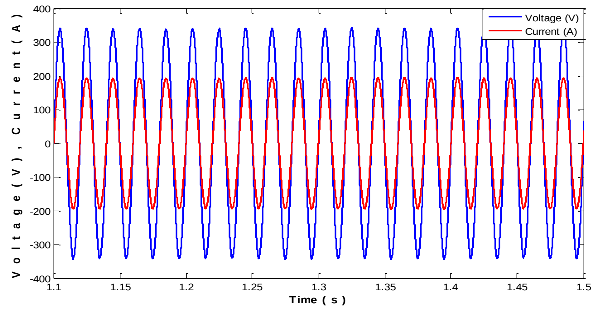

Fig. 14: PEDT Output voltage and current under voltage sag

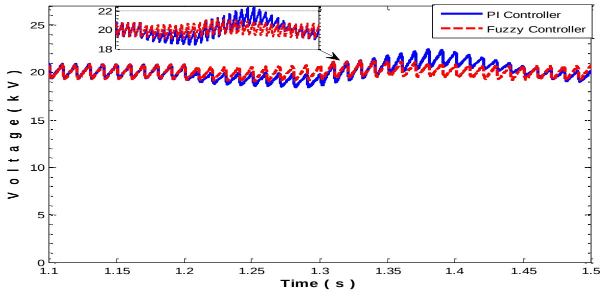

Fig. 15: PEDT High voltage DC-link under voltage sag

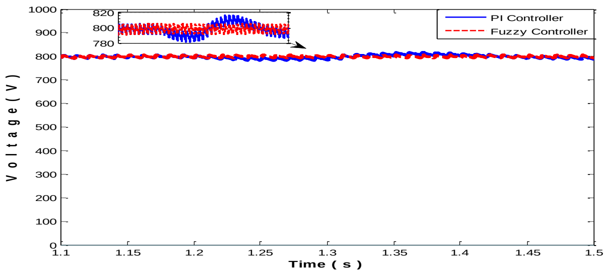

Fig. 16: PEDT Low voltage DC link under voltage sag

Table 4: Comparison between the FLC and the PI Controller when voltage sag applied

Parameter	FLC	PI controller
High DC link voltage peak overshoot	0.88 kV	2.52 kV
High DC link voltage peak undershoot	0.48 kV	0.63 kV
High DC link voltage setting time after the voltage sag	1.40 s	1.45 s
Low DC link voltage peak overshoot	0.2 V	13.5 V
Low DC link voltage peak undershoot	0 V	18.6 V

6. Conclusion

In this paper, a novel power electronic distribution transformer (PEDT) was introduced based on the fuzzy logic controller (FLC). The PEDT was developed by replacing the conventional PI controller with an FLC to improve the PEDT dynamic behaviours and improve the power quality. The proposed PEDT was tested under the steady-state and transient conditions, for the conventional PI and the proposed FLC. The FLC gives better dynamic response compared to the PI controller. The PEDT with FLC has less harmonic distortion (THD) of 1.98

% compared to the PI controller 2.24 % and the power factor was close to unity. The PEDT with the developed controller improved the power quality of the system, which can widen the application range of the PEDT.

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